REMARKS/ARGUMENTS

Reconsideration is requested in view of the following remarks. Claims 26 and 28 have been editorially revised. Support for the claim revisions can be found in paragraph 15 of the specification and Figures 1-3. Claims 26, 28 and 29 remain under consideration in the present application.

Claim Rejections – 35 USC §103

Claims 26, 28 and 29 stand rejected under 35 U.S.C. §103(a) as unpatentable over Biard (US 4,661,726). Applicant respectfully traverses this rejection.

Claim 26 has been editorially revised to more clearly and precisely claim what the Applicant regards as the invention. Specifically, claim 26 has been editorially revised to address specifics that were absent in the claims regarding how the first and second nodes structurally comprise "redistribution point(s) configured to recognize and transmit...BFL level-shifting/inverter circuit," as set forth in the Office action mailed July 31, 2007.

Claim 26 is directed to a buffered field effect transistor logic (BFL) level-shifting/inverter circuit comprising:

an inverter stage input;

an NMOS depletion mode inverter responsive to said inverter stage input to produce an inverted output;

a buffered field effect transistor logic (BFL) stage coupled to the inverted output and comprising a first NMOS depletion mode field effect transistor (FET) having a first gate and an associated first channel, a second NMOS depletion mode FET having a second gate and an associated second channel, and a voltage drop circuit electrically connected in series between said first channel and said second channel;

a first output at a first electrical node between said voltage drop circuit and said first channel, wherein said circuit is fabricated on a silicon carbide substrate; and

a second output at a second electrical node between said voltage drop circuit and said second channel, wherein said second electrical node is configured to transmit a chopping signal to a first chopping circuit other than said BFL level-shifting/inverter circuit in response to a clock input signal received at the inverter stage input, said first electrical node is configured to transmit a level-shifted chopping signal to a second chopping circuit other than said BFL level-shifting/inverter circuit in response to the clock input signal received at the inverter stage input, and wherein the level-shifted chopping signal is a level-shifted replica of the chopping signal generated by shifting a voltage level of the chopping signal, and further wherein the BFL level-shifting/inverter circuit comprises solely NMOS depletion mode based devices.

The invention of Biard is directed solely to a buffered FET logic (BFL) temperature compensation system for semiconductor logic gates where the temperature compensation is accomplished by depletion mode FET's in electrical series relationship (See column 4, lines 45-47, claims 1 and 26 of Biard). The theory of operation disclosed by Biard is directed solely to temperature compensation using gallium arsenide, indium arsenide or silicon technologies (See column 1, lines 58-60 of Biard).

In contradistinction, the claimed invention is directed to a BFL level-shifting/inverter circuit using silicon carbide (SiC) technology. More specifically, independent claims 26 and 29 both require the claimed BFL level-shifting/inverter circuit to be fabricated on a silicon carbide substrate. Paragraph [0020] of the specification describes that SiC circuits are capable operation at much higher temperatures than that achievable using conventional silicon technologies. At best, Biard only discloses use of conventional silicon technologies in column 1, lines 58-60 of Biard. The theory of operation of the invention of Biard thus bears no resemblance to the theory of operation of the claimed invention.

Further, the claimed invention requires two output nodes in which one output node is configured to transmit a chopping signal to a first chopping circuit in response to a clock input signal received at an inverter stage input while the other output node is

configured to transmit a level-shifted replica of the chopping signal to a second chopping circuit other than said BFL level-shifting/inverter circuit in response to the clock input signal received at the inverter stage input, and wherein the level-shifted replica of the chopping signal is generated by shifting a voltage level of the chopping signal. The temperature compensation circuit of Biard however discloses only a single temperature compensated output node. More specifically, the invention of Biard employs a temperature compensation circuit between the top transistor 32 and the bottom transistor 37 of a BFL circuit; while the claimed invention requires a level-shifting circuit between the top and bottom transistors, Q3 and Q4, of a BFL circuit.

The rejection asserts that a voltage drop or what is commonly called a level shifter is connected between the first and second transistors and is composed of elements like 33, 34 of Biard's Figure 4. The invention of Biard however, discloses only one output node, while the claimed invention requires two output nodes, each configured to transmit a chopping signal to a respective chopping circuit other than said BFL level-shifting/inverter circuit.

The invention of Biard cannot be modified as suggested in the rejection to arrive at the claimed invention without improperly using the claimed invention as a template since such a modification of the Biard invention would result in one temperature compensated output node and one additional output node that is not temperature compensated, thus defeating the purpose of the Biard temperature compensation invention. The resultant nodes suggested by the rejection would result in one output node that is not temperature compensated and one node that is temperature compensated, thus making it impossible to generate a replica of an output node signal as required by claim 26. Further, there is no motivation to modify the invention of Biard to provide two output nodes, each configured to transmit a chopping signal to a respective chopping circuit other than the BFL circuit in response to a clock input signal received at the inverter input.

Biard nowhere discloses or teaches the claimed BFL level-shifting/inverter circuit having a first output at a first electrical node between said voltage drop circuit and a first channel; and a second output at a second electrical node between said voltage drop circuit and a second channel, wherein said second electrical node is configured to transmit a chopping signal to a first chopping circuit other than said BFL level-shifting/inverter circuit in response to a clock input signal received at the inverter stage input, said first electrical node is configured to transmit a level-shifted chopping signal to a second chopping circuit other than said BFL level-shifting/inverter circuit in response to the clock input signal received at the inverter stage input, and wherein the level-shifted chopping signal is a level-shifted replica of the chopping signal generated by shifting a voltage level of the chopping signal because the theory of operation of the Biard invention is directed solely to a single temperature compensated output node that bears absolutely no resemblance to the claimed invention. The only motivation for modifying the invention of Biard is the claimed invention itself which is not a proper basis for modifying the invention of Biard.

Biard is also completely silent regarding technology such as SiC technology that is capable of operation at temperatures above 300 degrees Celsius as described in paragraph [0020] of the Applicant's specification. In fact, Biard specifically states in column 1, lines 19-25 that the disclosed invention provides a temperature compensation scheme that is capable of operation over a temperature range of -55 degrees Celsius to +125 degrees Celsius. The invention of Biard therefore has nothing whatsoever to do with SiC circuit technology such as required by the claimed invention.

The temperature compensation scheme disclosed by Biard is necessary to achieve operation of the BFL circuit over the -55 degrees Celsius to +125 degrees Celsius temperature range disclosed by Biard. In contradistinction, the claimed BFL level-shifting/inverter circuit is capable of operation above +300 degrees Celsius due to its claimed circuit topology and claimed use of SiC technology.

For at least these reasons, claim 26 and claim 28 that has corresponding patentable features, are patentable over Biard. Claim 29 is also patentable over Biard since it depends from claim 28 that is allowable. Applicant does not concede the correctness of the rejection.

Claim Rejections – 35 USC §103

Claims 28 and 29 are rejected under 35 U.S.C. §103(a) as unpatentable over Biard in view of Tohyama (US 4,810,907) and Alok (US 6,559,068). Applicant respectfully traverses this rejection for at least the same reasons discussed above regarding the rejection of claims 26, 28 and 29 in view of Biard.

Further, Alok discloses forming a gate oxide on a SiC substrate in the presence of metallic impurities to yield a MOSFET with improved inversion layer mobility. The invention of Alok is thus related to a single MOSFET device and is completely silent regarding circuit topologies comprising a plurality of MOSFET devices formed on a SiC substrate. Although Alok does disclose that SiC is an ideal semiconductor material for high temperature applications, Alok is also completely silent regarding BFL circuit functionality at high temperatures.

At best, Biard, Tohyama and Alok together teach a BFL gate utilizing a temperature compensation scheme to operate at high temperatures. In contradistinction, the claimed BFL circuit does not require temperature compensation to achieve the claimed level shifting.

For at least these reasons, claims 28 and 29 are patentable over Biard, alone or in combination with Tohyama and Alok. Neither Tohyama alone or in combination with Alok remedy the deficiencies of Biard that requires a first output at a first electrical node between said voltage drop circuit and said first channel, wherein said circuit is fabricated on a silicon carbide substrate; and a second output at a second electrical node between said voltage drop circuit and said second channel, wherein said second electrical node is configured to transmit a chopping signal to a first chopping circuit other than said BFL

level-shifting/inverter circuit in response to a clock input signal received at the inverter stage input, said first electrical node is configured to transmit a level-shifted chopping signal to a second chopping circuit other than said BFL level-shifting/inverter circuit in response to the clock input signal received at the inverter stage input, and wherein the level-shifted chopping signal is a level-shifted replica of the chopping signal generated by shifting a voltage level of the chopping signal, and further wherein the BFL level-shifting/inverter circuit comprises solely NMOS depletion mode based devices.

Applicant does not concede the correctness of the rejections or the relevance of Tohyama and Alok to the remaining claim features.

Favorable reconsideration in the form of a Notice of Allowance is requested. If the Examiner believes a telephone conference would advance the prosecution of this application, the Examiner is invited to telephone the undersigned at (507) 351-4450.

Respectfully submitted,

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